In the Claims

1. (Original) A plurality of capacitors embedded in a printed circuit structure, at least one of the plurality of capacitors comprising:

a first electrode overlaying a first substrate layer of the printed circuit structure;

a crystallized dielectric oxide core overlaying the first electrode, the crystallized dielectric oxide core having a thickness that is less than 1 micron and having a capacitance density greater than 1000 pF/mm^2, wherein the material and thickness are the same for each of the plurality of capacitors, and wherein the crystallized dielectric oxide core is isolated from crystallized dielectric oxide cores of all other capacitors of the plurality of capacitors;

a second electrode overlying the crystallized dielectric oxide core; and

a high temperature anti-oxidant layer disposed between and contacting the crystallized dielectric oxide layer and at least one of the first and second electrodes.

2. (Original) The plurality of capacitors according to claim 1, wherein the first crystallized dielectric oxide layer is formed from a dielectric oxide that contains lead.

3. (Original) The plurality of capacitors according to claim 1, wherein the first crystallized dielectric oxide layer is formed from a material that is selected from the group consisting of lead zirconate titanate, lead lanthanum zirconate titanate, lead calcium zirconate titanate, lead lanthanide titanate, lead titanate, lead zirconate, lead magnesium niobate, barium titanate, and barium strontium titanate, the crystallized dielectric oxide layer further comprising optional additional small quantities of nickel, niobium, calcium or strontium.

4. (Original) The plurality of capacitors according to claim 1, wherein the crystallized dielectric oxide core has a capacitance density greater than 2000 pF/mm^2.

5. (Original) The plurality of capacitors according to claim 1, wherein the first and second electrodes each comprise a metal selected from a group consisting of copper, copper alloys, nickel, and nickel alloys.

6. (Original) The plurality of capacitors according to claim 1, wherein the first and second electrodes are each less than 70 microns thick.

7. (Original) The plurality of capacitors according to claim 1, wherein the high temperature anti-oxidant layer comprises, by weight, more than 50% of one of palladium, platinum, iridium, and nickel or a combination thereof.

8. (Original) The plurality of capacitors according to claim 7, wherein the high temperature anti-oxidant layer further comprises no more than 49% by weight of one or more elements other than palladium, platinum, iridium, and nickel.

9. (Original) The plurality of capacitors according to claim 8, wherein the one or more elements other than palladium, platinum, iridium, and nickel are aluminum, chromium, and phosphorus.

10. (Original) A method for fabricating a plurality of capacitors embedded in a printed circuit structure, comprising:

fabricating a foil comprising a first electrode layer, a second electrode layer, a crystallized dielectric oxide layer disposed between the first electrode layer and the second electrode layer, and a high temperature anti-oxidation barrier between and contacting the crystallized dielectric oxide layer and at least one of the first and second electrode layers, wherein the crystallized dielectric oxide layer is less than 1 micron thick and has a capacitive density greater than 1000pF/mm^2;

adhering the first electrode layer of the foil to a printed circuit sub-structure;

selectively removing portions of the second electrode layer to form a top electrode of each of the plurality of capacitors and to form exposed portions of the crystallized dielectric oxide layer;

selectively removing portions of the crystallized dielectric oxide layer within the exposed portions thereof to form exposed portions of the first electrode layer; and

selectively removing portions of the first electrode layer within exposed portions thereof to form a bottom electrode of each of the plurality of capacitors.

11. (Original) The method for fabricating a plurality of capacitors according to claim 10, wherein selectively removing portions of the first electrode layer, further comprises forming the bottom

electrode beyond the area of the isolated dielectric core to provide an electrical connection to one of a plated via and a plated through hole.

12. (Original) The method for fabricating a plurality of capacitors according to claim 10, wherein selectively removing portions of the second electrode layer includes simultaneously removing an essentially coextensive portion of the high temperature anti-oxidation barrier.

13. (Currently Amended) The method for fabricating a plurality of capacitors according to claim ~~9~~10, wherein the portions of the crystallized dielectric oxide layer are selectively removed by one of abrasion and laser scribing.

14. (Currently Amended) The method for fabricating a plurality of capacitors according to claim ~~9~~10, wherein selectively removing portions of the crystallized dielectric oxide layer further comprises placing a pattern of material to protect portions of the first electrode layer and the crystallized dielectric oxide layer that are not to be removed.

15. (Currently Amended) The method for fabricating a plurality of capacitors according to claim ~~9~~10, wherein selectively removing portions of the first electrode layer and selectively removing portions of the second electrode layer each comprise a photolithograhic chemical etching process.

16. (Currently Amended) The method for fabricating a plurality of capacitors according to claim ~~9~~10, wherein the crystallized dielectric oxide layer has a capacitance density greater than 2000 pF/mm^2.

17. (Currently Amended) The method for fabricating a plurality of capacitors according to claim ~~9~~10, wherein the first and second electrode layers each comprise a metal selected from a group consisting of copper, copper alloys, nickel, and nickel alloys.

18. (Currently Amended) The method for fabricating a plurality of capacitors according to claim ~~9~~10, wherein the first and second electrodes are each less than 25 microns thick.

19. (Currently Amended) The method for fabricating a plurality of capacitors according to claim 810, wherein the high temperature anti-oxidation barrier comprises, by weight, more than 50% of one of palladium, platinum, iridium, and nickel or a combination thereof.

20 (Currently Amended) The method for fabricating a plurality of capacitors according to claim 19, wherein the high temperature anti-oxidation barrier further comprises, by weight, no more than 49% of one or more elements other than palladium, platinum, iridium, and nickel.

21. (Currently Amended) The method for fabricating a plurality of capacitors according to claim 20, wherein the one or more elements other than palladium, platinum, iridium, and nickel are aluminum, chromium, and phosphorus.

22. (Original) A plurality of capacitors embedded in a printed circuit structure, the plurality of capacitors comprising:

a patterned first electrode overlaying a first substrate layer of the printed circuit structure;

a patterned crystallized dielectric oxide core overlaying the patterned first electrode, the patterned crystallized dielectric oxide core having a thickness that is less than 1 micron and having a capacitance density greater than 1000 pF/mm^2;

a patterned second electrode overlying the patterned crystallized dielectric oxide core; and

a patterned high temperature anti-oxidant layer disposed between and contacting the patterned crystallized dielectric oxide core and at least one of the patterned first and second electrodes.

23. (Original) The plurality of capacitors embedded in a printed circuit structure according to claim 22, wherein the patterned second electrode is within boundaries of the patterned crystallized dielectric oxide core, which is within boundaries of the patterned first electrode.

24. (Original) The plurality of capacitors embedded in a printed circuit structure according to claim 22, wherein the patterned first electrode includes at least one clearance annulus that is exposed by the patterned crystallized dielectric oxide core, wherein the at least one clearance annulus provides clearance for a plated through hole that does not contact the patterned first electrode.

25. (Original) The plurality of capacitors embedded in a printed circuit structure according to claim 22, wherein the patterned first electrode includes at least one area that is a bottom electrode for only one capacitor and a corresponding at least one contiguous area that is exposed by the patterned crystallized dielectric oxide core, wherein the corresponding at least one contiguous area provides for connection to a blind via.

26. (Original) An electronic device, comprising:

a printed circuit board comprising

an embedded capacitor that is one of a plurality of capacitors embedded in a particular layer of the printed circuit board, comprising

a first electrode overlaying a first substrate layer of the printed circuit board,

a crystallized dielectric oxide core overlaying the first electrode, the crystallized dielectric oxide core having a thickness that is less than 1 micron and having a capacitance density greater than 1000 pF/mm^2, wherein the material and thickness are the same for each of the plurality of capacitors, and wherein the crystallized dielectric oxide core is isolated from crystallized dielectric oxide cores of all other capacitors of the plurality of capacitors,

a second electrode overlying the crystallized dielectric oxide core, and

a high temperature anti-oxidant layer disposed between and contacting the crystallized dielectric oxide layer and at least one of the first and second electrodes; and

at least one electronic component, wherein the first and second electrodes are connected to terminals of the at least one electronic component; and

a power supply that is coupled to at least one of the at least one electronic component.